ABSTRACT

SWITCHED-CURRENT ANALOGUE-TO-DIGITAL CONVERTER

An current mode analogue-to-digital converter uses a conversion stage which operates using a two-phase clock and which requires the input signal to be present during only one of the phases. A sample-and-hold circuit (120, 130, 135) samples the input signal during the first clock phase and during the second clock phase a quantised bit value is generated from a mirror of the held input current by a kickback-free comparator circuit (140). Also during the second clock phase a residue is generated using the quantised value and a non-mirrored version of the held input current. Optionally, two comparator circuits (140, 140″) may be used to provide two-level quantisation, enabling errors introduced by the current mirror to be corrected by a Redundant Signed Digit algorithm. Two pipelines of conversion stages (S_i', S_i'') can be multiplexed to double the conversion rate.

(Figure 3)